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ABSTRACT OF THE INVENTION

The present invention relates to a method for forming an isolation trench structure in a semiconductor substrate without causing deleterious topographical depressions in the upper surface thereof which cause current and charge leakage to an adjacent active area. The inventive method forms a pad oxide upon a semiconductor substrate, and then forms a nitride layer on the pad oxide. The nitride layer is patterned with a mask and etched to expose a portion of the pad oxide layer and to protect an active area in the semiconductor substrate that remains covered with the nitride layer. A second dielectric layer is formed substantially conformably over the pad oxide layer and the remaining portions of the first dielectric layer. A spacer etch is then carried out to form a spacer from the second dielectric layer. The spacer is in contact with the remaining portion of the first dielectric layer. An isolation trench etch follows the spacer etch. An optional thermal oxidation of the surfaces in the isolation trench may be performed, which may optionally be followed by doping of the bottom of the isolation trench to further isolate neighboring active regions on either side of the isolation trench. A conformal layer is formed substantially conformably over the spacer, over the remaining portions of the first dielectric layer, and substantially filling the isolation trench. Planarization of the conformal layer follows, either by CMP or by etchback or by a combination thereof. An isolation trench filled with a structure results. The resulting structure has a flange and shaft, the cross section of which has a nail shape in cross section.

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